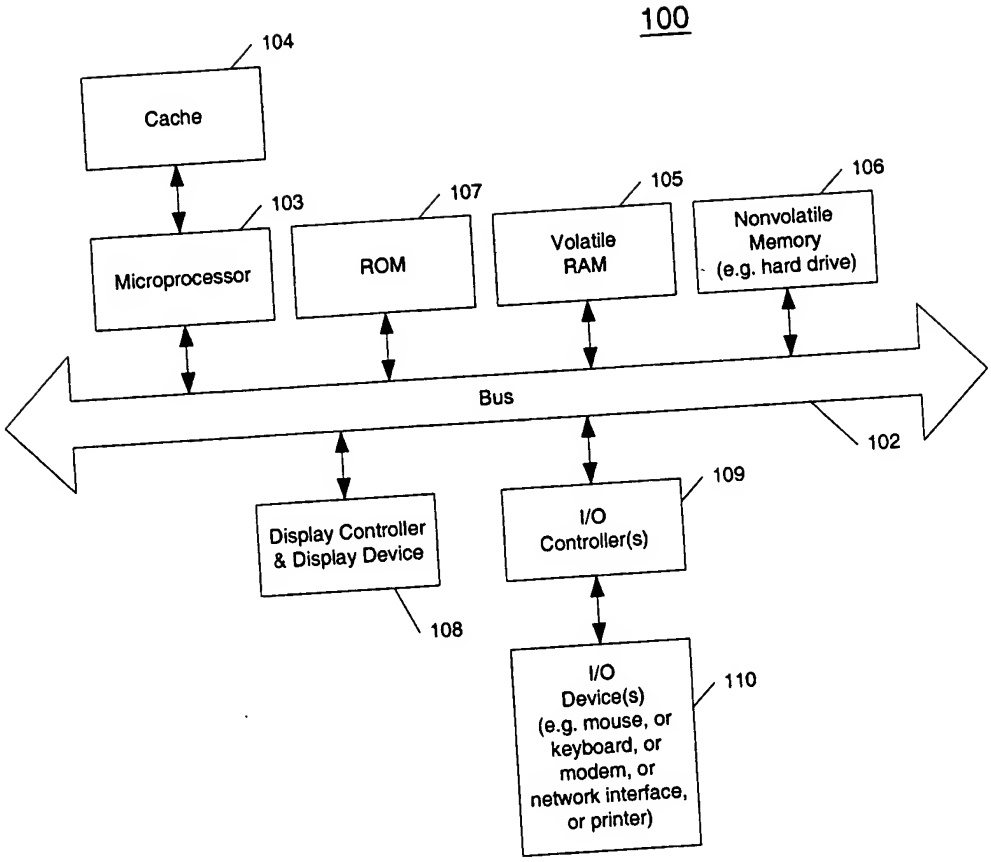
100
104
Cache
103
Microprocessor
107
ROM
105
Volatile
RAM
106
Nonvolatile
Memory
(e.g. hard drive)
Bus
102
Display Controller
& Display Device
108
109
I/O
Controller(s)
I/O
Device(s)
(e.g. mouse, or
keyboard, or
modem, or
network interface,
or printer)
110

Fig. 1

200

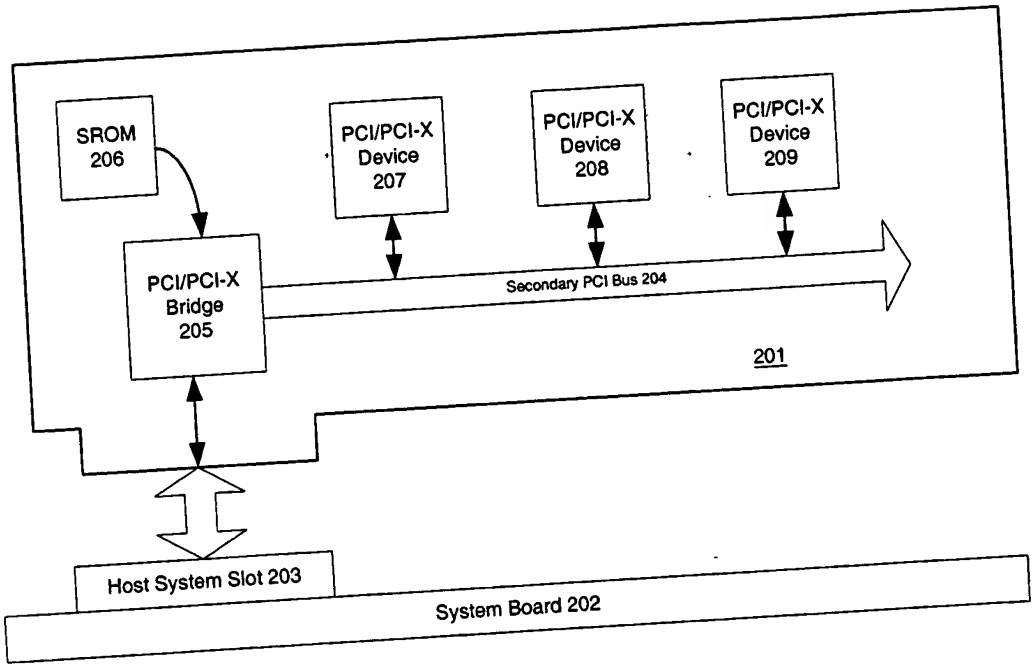
SROM
206
PCI/PCI-X
Device
207
PCI/PCI-X
Device
208
PCI/PCI-X
Device
209
PCI/PCI-X
Bridge
205
Secondary PCI Bus 204
201
Host System Slot 203
System Board 202

Fig. 2

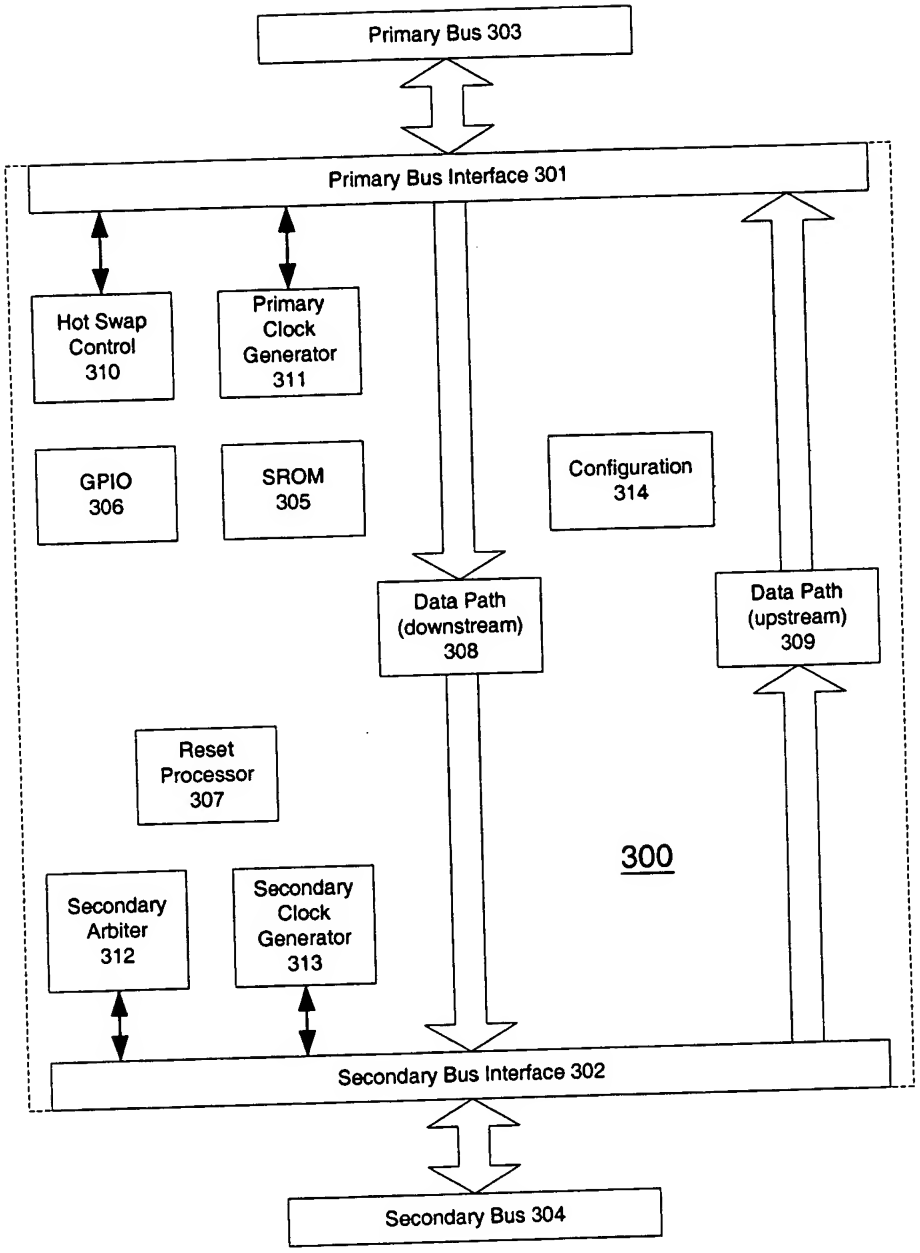
Primary Bus 303
Primary Bus Interface 301
Hot Swap Control 310
Primary Clock Generator 311
GPIO 306
SROM 305
Configuration 314
Data Path (downstream) 308
Data Path (upstream) 309
Reset Processor 307
300
Secondary Arbiter 312
Secondary Clock Generator 313
Secondary Bus Interface 302
Secondary Bus 304

Fig. 3

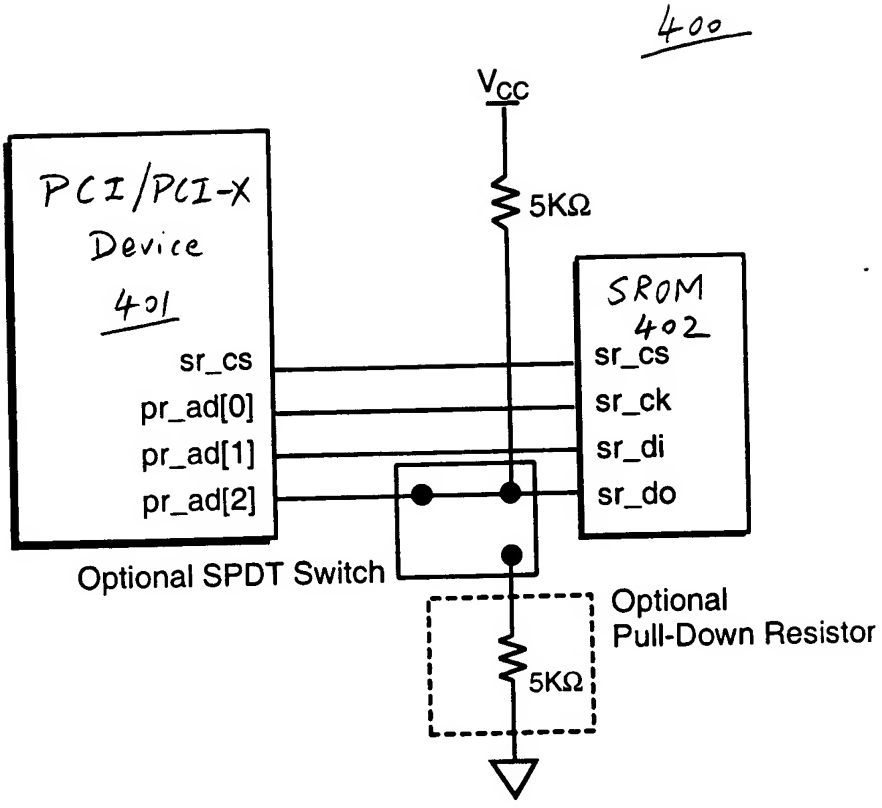
400
V_{CC}
5KΩ
PCI/PCI-X
Device
401
sr_cs
pr_ad[0]
pr_ad[1]
pr_ad[2]
SROM
402
sr_cs
sr_ck
sr_di
sr_do
Optional SPDT Switch
Optional
Pull-Down Resistor
5KΩ

Fig. 4

Byte offset	Description
00h	[7:6] 10b to enable serial pre-load [5:0] 000001b (load Vendor ID/Device ID/Revision ID) [5:0] 000000b (Reserved)
01h	Arbiter Control / Status[7:0]
02h	Arbiter Control / Status[15:8]
03h	31154 Control Register 0
04h	31154 Control Register 1[7:0]
05h	31154 Control Register 1[15:8]
06h	31154 Control Register 2[7:0]
07h	31154 Control Register 2[15:8]
08h	Multi-Transaction Timer Register[7:0]
09h	Multi-Transaction Timer Register[15:8]
0Ah	Pre-Fetch Policy Register[7:0]
0Bh	Pre-Fetch Policy Register[15:8]
0Ch	P_SERR# Assertion Control Register[7:0]
0Dh	P_SERR# Assertion Control Register[15:8]
0Eh	Secondary IDSEL Select Register[7:0]
0Fh	Secondary IDSEL Select Register[15:8]
10h	Secondary IDSEL Fnct 0 Enable Register[7:0]
11h	Secondary IDSEL Fnct 0 Enable Register[15:8]
12h	GPIO Pin Configuration Register
13h	GPIO Write One to Toggle Register
14h	Opaque Memory Base and Limit Register[7:0]
15h	Opaque Memory Base and Limit Register[15:8]
16h	Opaque Memory Base and Limit Register[23:16]
17h	Opaque Memory Base and Limit Register[31:24]
18h	Opaque Memory Base Upper 32 Bits[7:0]
19h	Opaque Memory Base Upper 32 Bits[15:8]
1Ah	Opaque Memory Base Upper 32 Bits[23:16]
1Bh	Opaque Memory Base Upper 32 Bits[31:24]
1Ch	Opaque Memory Limit Upper 32 Bits[7:0]
1Dh	Opaque Memory Limit Upper 32 Bits[15:8]
1Eh	Opaque Memory Limit Upper 32 Bits[23:16]
1Fh	Opaque Memory Limit Upper 32 Bits[31:24]
20h	Slot Number Register
21h	Chassis Number Register
22h	Power Management Next Item Pointer: Must be pre-loaded with a value of E4h to expose VPD register block to software.
23h	Power Management Capabilities Register[15:8] This register may be pre-loaded with high order bits [15:11] set to 11111b indicating that the bridge supports PME# generation from any PM DState. This feature may be used to workaround a Windows 98 bridge power management errata.
24h	ID [7:0] The Device ID and Vendor ID are only preloaded if SROM offset 00h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
25h	ID [15:8].
26h	ID [23:16].
27h	ID [31:24].
28	RID The Revision ID is only preloaded if SROM offset 00h = 1000_0001. Otherwise, offsets 24h-28h are ignored.
29h - 7Fh	Reserved.
80h - 0FFh	Vital Product Data (Read Only region).
100h - 1FFh	Vital Product Data (Read / Write region).

501

500

Fig. 5

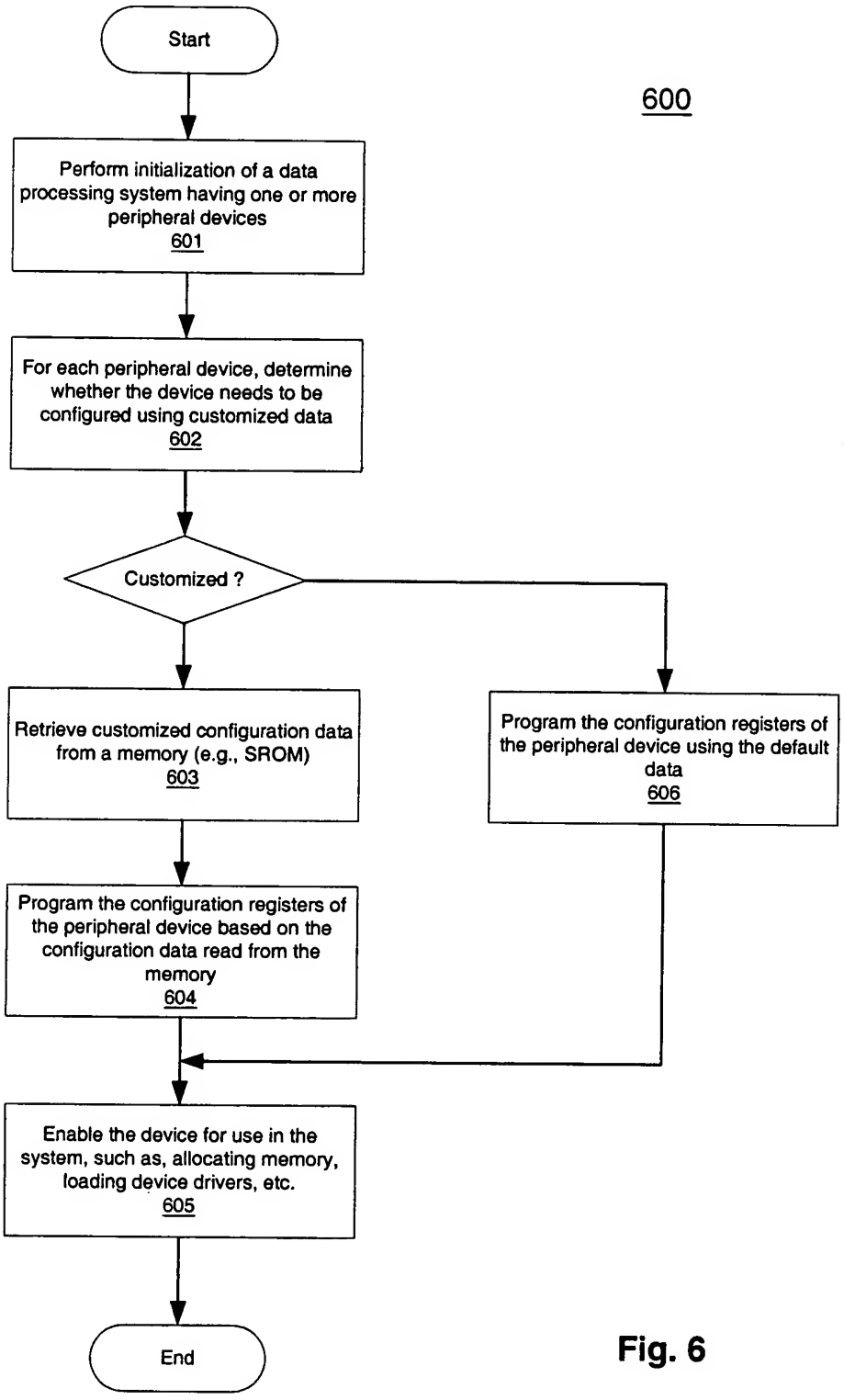
600
Start
Perform initialization of a data processing system having one or more peripheral devices
601
For each peripheral device, determine whether the device needs to be configured using customized data
602
Customized ?
Retrieve customized configuration data from a memory (e.g., SROM)
603
Program the configuration registers of the peripheral device based on the configuration data read from the memory
604
Program the configuration registers of the peripheral device using the default data
606
Enable the device for use in the system, such as, allocating memory, loading device drivers, etc.
605
End

Fig. 6